REMARKS

Claims 52-54 have been added. Claims 1, 14 and 26 have been amended. Claims 49-51 have been withdrawn. Claims 1-3, 6-11, 14-16, 20, 22-24 and 26-34 are pending. Applicant reserves the right to pursue the original claims and other claims in this and in other applications.

Claims 1-3, 6-11, 14-16, 20, 22-24 and 26-33 stand rejected on the grounds of nonstatutory obviousness-type double patenting over claims 1-6, 12, 14-16, 18 and 36-40 of U.S. Patent No. 7,154,136. Applicant respectfully traverses the rejection.

Applicant notes that in this Amendment and during subsequent prosecution, the claims of the present application may be amended to make this rejection moot. Additionally, Applicant notes that the claims can be fully considered now without this issue being immediately addressed. As such, Applicant respectfully requests that the double patenting rejection be held in abeyance until allowable subject matter is indicated, or that the rejection be withdrawn.

Claims 1-3, 6, 7, 11, 14-16, 20 and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by JP 63-9968 ("Yoshinori"). Applicant respectfully traverses the rejection.

Claim 1 recites an image sensor comprising "a plurality of pixel cells formed within said substrate, each pixel cell comprising a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first region of a first conductivity type; and a plurality of trenches, each trench being provided along a perimeter of a respective pixel

cell, each trench extending at least to a surface of the base layer and below a lower level of said charge collection region, each trench having sidewalls, and being at least partially filled with a material that inhibits electrons from passing through said trench, wherein each of said plurality of trenches prevents diffusion of photo-generated charge collected by said photo-conversion device in one pixel cell to an adjacent pixel cell." Yoshinori does not teach or suggest all of the limitations of claim 1.

The Yoshinori device has a substrate 1 doped with N-type impurity, an epitaxial layer 2, and a plurality of trenches. (Yoshinori, Abstract; Figure 7). The Office Action cites to Figures 1-7 and particularly to Figure 6 of Yoshinori to contend that Yoshinori discloses all of the limitations of claim 1. (Office Action, p.4). Applicant respectfully disagrees. The Yoshinori device has trenches dug to the substrate on which the epitaxial layer 2 is shaped. (Yoshinori, Abstract; Figure 7). In contrast, the trenches 202 in the claimed invention are formed in the substrate 200 and they extend to the surface of the base layer 201 and below a lower level of said charge collection region. (Present Application, Figures 2-6). Further, the trenches in the Yoshinori device are formed between p-n-p transistors. (Yoshinori, Figure 7).

In contrast, the image sensor of the claimed invention has plurality of pixel cells, "each pixel cell comprising a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first region of a first conductivity type . . . wherein each of said plurality of trenches prevents diffusion of photo-generated charge collected by said photo-conversion device in one pixel cell to an adjacent pixel cell." Because Yoshinori does not disclose or teach all of the limitations, Applicant respectfully requests that the rejection of

independent claim 1 and its dependent claims 2-3, 6, 7 and 11 be withdrawn and the claims allowed.

Claim 14 recites a structure for isolating an active area on a semiconductor device comprising "a doped charge collection region of a second conductivity type for accumulating charge formed in said active area below a first region of a first conductivity type; a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, wherein said trench extends at least to a surface of a base layer below said substrate which is below a lower level of said charge collection region, and wherein said trench has sidewalls; a dielectric liner formed along said sidewalls; and a material formed over said dielectric liner that at least partially fills said trench and inhibits electrons from passing through said trench, wherein said trench prevents diffusion of electrons from said doped charge collection region into a region outside said active area."

As mentioned above, the Yoshinori device has trenches between p-n-p transistors. (Yoshinori, Figure 6). In contrast, the claimed invention has a "doped charge collection region of a second conductivity type for accumulating charge formed in [the] active area" and the trench 202 "extends at least to a surface of a base layer below said substrate which is below a lower level of said charge collection region [and] prevents diffusion of electrons from said doped charge collection region into a region outside said active area." (Present Application, ¶¶ [0030]-[0031]; Figures 2-6). Yoshinori fails to disclose or teach all of the limitations of claim 14. Therefore, Applicant requests that the rejection of independent claim 14 and dependent claims 15, 16, 20 and 24 be withdrawn and the claims allowed.

Claims 26-29 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshinori. Applicant respectfully traverses the rejection.

Claim 26 recites a processing system comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, the active area having a charge collection region of n-type conductivity for accumulating charge and located below a p-type region of said active area, wherein said trench extends at least to a surface of a base layer below said substrate and to a level below a lower level of said charge collection region, and wherein said trench has sidewalls and inhibits diffusion of charge outside said active area."

As mentioned earlier, the Yoshinori device has trenches between p-n-p transistors. (Yoshinori, Figure 6). In contrast, in the claimed invention, the "active area [has] a charge collection region of n-type conductivity for accumulating charge" and the trench 202 "extends at least to a surface of a base layer below said substrate and to a level below a lower level of said charge collection region [and] inhibits diffusion of charge outside said active area." (Present Application, ¶¶ [0030]-[0031]; Figures 2-6). Because Yoshinori fails to disclose or teach all of the limitations of claim 26, Applicant submits that the rejection of independent claim 26 and dependent claims 27-29 and 33 should be withdrawn and the claims allowed.

Claims 8, 9, 22, 23, 30 and 31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yoshinori in view of U.S. Publication No. 2004/0227061 ("Clevenger"). Applicant respectfully traverses the rejection.

Claims 8 and 9 depend from claim 1 and as such, recite an image sensor, comprising, in part, "a photo-conversion device having a charge collection region of a second conductivity type for accumulating photo-generated charge formed in said substrate below a first region of a first conductivity type; and a plurality of trenches . . . wherein each of said plurality of trenches prevents diffusion of photo-generated charge collected by said photo-conversion device in one pixel cell to an adjacent pixel cell."

Claims 22 and 23 depend from claim 14 and as such, recite a structure for isolating an active area on a semiconductor device comprising, in part, "a doped charge collection region of a second conductivity type for accumulating charge formed in said active area below a first region of a first conductivity type; a trench formed in a substrate . . . wherein said trench prevents diffusion of electrons from said doped charge collection region into a region outside said active area."

Claims 30 and 31 depend from claim 26 and as such, recite a processor system comprising, in part, "a trench formed in a substrate along at least a portion of a periphery of said active area in said semiconductor device, the active area having a charge collection region of n-type conductivity for accumulating charge and located below a p-type region of said active area, wherein said trench extends at least to a surface of a base layer below said substrate and to a level below a lower level of said charge collection region, and wherein said trench has sidewalls and inhibits diffusion of charge outside said active area."

As mentioned earlier, Yoshinori fails to teach or disclose all of the limitations of claims 1, 14 and 26. Clevenger fails to cure the deficiencies of Yoshinori. The Office Action relies on Clevenger to only teach a trench depth greater than about 2000 Angstroms and a

CMOS image sensor. (Office Action, pp. 7-8). Therefore, Applicant respectfully requests that the rejection of claims 8, 9, 22, 23, 30 and 31 be withdrawn and the claims allowed.

Claims 52-54 depend from claim 1 and therefore, contain all of the limitations of claim 1. For the reasons mentioned earlier and for other reasons, claims 52-54 are allowable.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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